Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.090”**

**PAD FUNCTION:**

1. **VL+**
2. **OUT 1**
3. **–IN 1**
4. **+IN 1**
5. **V-**
6. **+IN 2**
7. **–IN 2**
8. **OUT 2**
9. **VL-**
10. **OUT 3**
11. **–IN 3**
12. **+IN 3**
13. **V+**
14. **+IN 4**
15. **–IN 4**
16. **OUT 4**

**7 8 9 10 11**

**3 2 1 16 15**

**14**

**13**

**12**

**4**

**5**

**6**

**.102”**

**NOTES:**

**Chip back should be connected to V-**

**This device has been fabricated with gold back metal or unplated**

**(bare silicon.) Either backside finish may be supplied.**

**Top Material: Al**

**Backside Material: Si or Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: 3909A**

**APPROVED BY: DK DIE SIZE .090” X .102” DATE: 8/25/21**

**MFG: HARRIS / INTERSIL THICKNESS .019” P/N: HA0-4902-2**

**DG 10.1.2**

#### Rev B, 7/19/02